CLAIMS

What is claimed is:

1. A method comprising:

receiving an interrupt message from a device via a shared interrupt interface;

checking one or more registers to identify the device; and

transmitting an indication of the interrupt message to one or more selected operating entities based on the identity of the device.

2. The method of claim 1 wherein the one or more selected operating entities comprises one or more virtual machines.

3. The method of claim 1 wherein the one or more selected operating entities comprises threads in a multi-threaded operating environment.

4. The method of claim 1 wherein the one or more registers comprise at least one Peripheral Component Interconnect (PCI) Status register for one or more corresponding devices.

5. The method of claim 4 wherein the PCI Status register conforms to the PCI Bus Standard, Version 2.3 or higher.

6. The method of claim 4 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

7. The method of claim 1 wherein the one or more virtual machines comprise virtual machines that registered to have access to the identified device.

8. The method of claim 1 further comprising executing an interrupt service routine chain with each of the one or more virtual machines.

9. The method of claim 1 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.

10. The method of claim 1 wherein transmitting an indication of the interrupt message to one or more virtual machines based on the identity of the device comprises transmitting an identity of the device.

11. An article comprising a computer-accessible medium having stored thereon instructions that, when executed, cause one or more processors to:

receive an interrupt message from a device via a shared interrupt interface;

check one or more registers to identify the device; and

transmit an indication of the interrupt message to one or more selected operating entities based on the identity of the device.

12. The article of claim 11 wherein the one or more selected operating entities comprises one or more virtual machines.

13. The article of claim 11 wherein the one or more selected operating entities comprises threads in a multi-threaded operating environment.

14. The article of claim 11 wherein the one or more registers comprise at least one Peripheral Component Interconnect (PCI) Status register for one or more corresponding devices.

15. The article of claim 14 wherein the PCI Status register conforms to the PCI Bus Standard, Version 2.3 or higher.

16. The article of claim 14 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

17. The article of claim 11 wherein the one or more virtual machines comprise virtual machines that registered to have access to the identified device.

18. The article of claim 11 further comprising instructions that, when executed cause the one or more processors to execute an interrupt service routine chain with each of the one or more virtual machines.

19. The article of claim 11 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.

20. The article of claim 11 wherein the instructions that cause the one or more processors to transmit an indication of the interrupt message to one or more virtual machines based on the identity of the device comprise instructions that, when executed, cause the one or more processors to transmit an identity of the device.

21. An apparatus comprising:

a plurality of virtual machines having associated respective operating systems;

a host monitor communicatively coupled with the plurality of virtual machines and coupled to receive an interrupt signal via a shared interrupt interface, wherein the host monitor reads a value stored in one or more registers corresponding to devices that asserted the interrupt signal to identify the device, and further wherein the host monitor selectively invokes an interrupt service signal to each of the plurality of virtual machines associated with the device asserting the interrupt signal.

22. The apparatus of claim 21 wherein the one or more registers comprise at least one Peripheral Component Interconnect (PCI) Status register for one or more corresponding devices.

23. The apparatus of claim 22 wherein the PCI Status register conforms to the PCI Bus Standard, Version 2.3 or higher.

24. The apparatus of claim 22 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

25. The apparatus of claim 21 wherein each virtual machine receiving the interrupt service signal from the host monitor executes at least one interrupt service routine.

26. The apparatus of claim 21 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.

27. The apparatus of claim 21 wherein the interrupt service signal comprises an identifier of the device.

28. A system comprising:

a memory controller; and

an article communicatively coupled with the memory controller, the article comprising a computer-accessible medium having stored thereon instructions that, when executed, cause one or more processors to receive an interrupt message from a device via a shared interrupt interface, check one or more registers to identify the device, and transmit an indication of the interrupt message to one or more operating entities based on the identity of the device.

29. The system of claim 28 wherein the one or more selected operating entities comprises one or more virtual machines.

30. The system of claim 28 wherein the one or more selected operating entities comprises threads in a multi-threaded operating environment.

31. The system of claim 28 wherein the one or more registers comprise at least one Peripheral Component Interconnect (PCI) Status register for one or more corresponding devices.

32. The system of claim 31 wherein the PCI Status register conforms to the PCI Bus Standard, Version 2.3 or higher.

33. The system of claim 31 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

34. The system of claim 28 further comprising instructions that, when executed cause the one or more processors to execute an interrupt service routine chain with each of the one or more virtual machines.

35. The system of claim 28 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.